REMARKS

I. Claim Rejections - 35 USC § 103

Requirements for Prima Facie Obviousness

The obligation of the examiner to go forward and produce reasoning and evidence in support of obviousness is clearly defined at M.P.E.P. §2142:

> "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

The U.S. Supreme Court ruling of April 30, 2007 (*KSR Int'l v. Teleflex Inc.*) states:

> "The TSM test captures a helpful insight: A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. Although common sense directs caution as to a patent application claiming as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the art to combine the elements as the new invention does."
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> "To facilitate review, this analysis should be made explicit."

The U.S. Supreme Court ruling states that it is important to identify a *reason* that would have prompted a person to combine the elements and to make that analysis *explicit*. MPEP §2143 sets out the further basic criteria to establish a *prima facie* case of obviousness:

1. a reasonable expectation of success; and

2. the teaching or suggestion of <u>all</u> the claim limitations by the prior art reference (or references when combined).

It follows that in the absence of such a *prima facie* showing of obviousness by the Examiner (assuming there are no objections or other grounds for rejection) and of a *prima facie* showing by the Examiner of a *reason* to combine the references, an applicant is entitled to grant of a patent. Thus, in order to support an obviousness rejection, the Examiner is obliged to produce evidence compelling a conclusion that the basic criterion has been met.

Biemond et al. in view of Nash et al.

The Examiner rejected claims 1, 7, and 14 under 3S U.S.C. §103(a) as being unpatentable over Biemond et al. ("Iterative Methods for Image Deblurring"), hereinafter referred to as "Biemond", in further view of Nash et al. ("VLSI Implementation of a Linear Systolic Array"), hereinafter referred to as "Nash".

Regarding claim 1, the Examiner argued that Biemond in view of Nash discloses a method of deblurring an image, comprising the steps of: downloading a blurred image having pixels into a systolic array processor, said processor comprising an array of processing logic blocks in parallel such that groups of pixel arrive in respective processing logic blocks; sequentially exchanging data between processing logic blocks by interconnecting each processing logic block with a predefined number of the processing logic blocks adjacent thereto; and uploading the deblurred image.

The Examiner argued that Biemond discloses an iterative method/or image deblurring performed by a computing system. The Examiner argued that Biemond describes the method used to process the image but does not explicitly teach the downloading of the image or the use of a systolic array processor to perform the deblurring method. The Examiner took official notice that the downloading of the image for processing is notoriously well known in the art, and is in fact an intrinsic step of an image processing method that augments an existing image. The

Examiner argued that Nash teaches the use of a systolic array for linear processing, and (the Examiner cited Nash 2nd paragraph on page 1) that the systolic array is broken down into processing elements (processing logic blocks). The Examiner argued that it would have been obvious to one of ordinary skill in the art to combine the teaching of Nash and Biemond to increase the processing performance of the system as is disclosed by Nash in the abstract. Furthermore, The Examiner argued that deblurring of images is disclosed as an application of the systolic array for on page 3 of Nash under the section entitled "Applications" and as further evidenced by Owens ("Computer Vision of the MGAP") in section 3.1 that the use of systolic algorithms (such as deblurring) for computer vision on an array processor (array processors perform parallel processing) was known to one of ordinary skill in the art.

The Examiner argued that Nash discloses (citing Nash in the section entitled "Linear Array Organization") the interconnection of the .processing elements. Also, The Examiner argued that further arrangements of processing element interconnections were known as is evidenced by Amin ("PVM Implementations for Low-Level Image Processing Systolic Array Designs"). Furthermore, The Examiner argued that a systolic array processor such as is taught by Nash (citing Nash paragraphs 5 and 6 of page 1393) is used to concurrently (i.e. in parallel) perform similar operations and then shift this processed data to a next set of processing elements (the Examiner cited data processing units, CPUs, ..., etc ...) wherein a next linear manipulation is performed on the data.

The Examiner admitted that Nash and Biemond do not explicitly teach the uploading of the blurred image. The Examiner took official notice that the uploading of the deblurred (processed) image is notoriously well known in the art. The Examiner argued that since the purpose of deblurring the image is to produce a deblurred image for display or further processing, it would have been obvious to

one of ordinary skill in the art to store or upload the processed image for retrieval or display.

The Examiner stated that claims 7 and 14 claim the corresponding device that performs the method of claim 1. The Examiner argued that as per the rejection of claim 1, the device of claims 7 and 14 has been disclosed in Biemond in view of Nash.

The Applicant respectfully disagrees with this assessment and notes that claims 1, 7 and 14 have been amended with this paper. Claim 1 is shown, for example, as follows:

> A method of deblurring a video image, comprising the steps of:
> downloading a blurred video image comprising a plurality of pixels into a systolic array processor, said systolic array processor comprising an array of processing logic blocks in parallel such that groups of said plurality of pixels arrive in each processing logic block of said array of processing logic blocks respectively;
> sequentially exchanging data between said array of processing logic blocks by interconnecting said each processing logic block with only a predefined number of processing logic blocks adjacent thereto;
> providing an iterative update of said blurred video image by storing each pixel of said plurality of pixels in three planes within said systolic array processor wherein said iterative update occurs within a video frame update rate of said blurred video image; and
> uploading a deblurred video image.

The Applicant notes that all 20 claims have been amended to standardize the language throughout the claims. Regarding claims 1, 7 and 14, the Applicant notes that the substantive amendments to the claims include the following additional limitations:

1) the image is a *video* image;

2) each processing block exchanges data *only* with adjacent processing blocks;

3) the iterative update stores each pixel of the image in three planes within the systolic array processor; and

4) the iterative update occurs within a video frame update rate of the video image.

The Applicant's paragraph [0019] discloses that the method concerns a deblurring method of *video* images; paragraph [0035] discloses the limitation of each processing block exchanges with *only* an adjacent block; the three planes limitation is disclosed in FIG. 1 and in paragraph [0034]; and paragraph [0036] discloses the iterations occur within a video frame update rate.

Biemond in view of Nash does not disclose these limitations. Biemond discloses methods of deblurring an image, but does not disclose that the image is a *video* image. Furthermore, Biemond does not disclose that the iteration update occurs within the video frame update rate. The Applicant has disclosed in the "Background" section that prior art deblurring methods and algorithms have a significant delay in the processing which is acceptable for static images, such as disclosed in Biemond; however, this delay would be unacceptable in streaming digital video images in real time, as disclosed in the Applicant's paragraph [0003] as follows:

> [0003] The existing deblurring algorithms and methods require significant computing power and deblurring of high resolution image would take some time even for modern powerful computers. While this processing time delay is often acceptable for deblurring static images, such as astronomical images, it makes it difficult or impossible to enhance streaming images--such as digital video--in real-time, at the frame update rate.

The Applicant's invention allows the streaming video image to be processed within the video frame update rate with the use of a systolic array processor. The Examiner has cited Nash for the disclosure of the systolic array processor and the interconnections of the processor, but has not cited how this discloses the limitation of "sequentially exchanging data between processing logic blocks by interconnecting each processing logic block with a predefined number of processing logic blocks *adjacent* thereto". The Applicant has amended to the claims to include the limitation

wherein the exchange of data is *only* with adjacent processing blocks. This is disclosed in the Applicant's paragraphs [0019] and [0035] as follows:

> [0019] The update, using the local feedback operators is implemented by using a systolic array processor, where each process can be mass-produced and is capable of simple multiplication and addition operations, as well as communication with the neighbors. With the localized operators, a parallelized implementation of the update algorithms is possible that is completely scalable to very large image sizes. Since the feedback operators are localized, *the data exchange necessary to perform the update computations is limited to a neighborhood of each array node processor* and computations do not depend on the image size. The proposed update being implemented on an inexpensive systolic processor enables real-time deblurring of high-resolution video images.
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> [0035] The update u(n+1)=u(n)-K*(H*u(n)-y.sub.b)-S*u(n) is amenable to a systolic array processor implementation. Such processor illustrated in FIG. 2 consists of an array of simple processing elements (logic blocks), one per image pixel The processing logic blocks are interconnected such that each can exchange data with its *immediate* neighbors. Each of the processing logic blocks also has some local data memory and is capable of simple arithmetic operations such as addition, subtraction, and multiplication. Using the interconnect logic, the blurred image can be downloaded into the processor array, each pixel into a respective processing logic block. *By sequentially exchanging data with the nearest neighbors, each logic block can accumulate data from any predefined number of neighbors within certain reach*. Of course this would require multiple update cycles, a larger number of cycles for a larger reach. (emphasis added)

Nash does indeed disclose a systolic array processor, but does not disclose a video image iteration wherein the processing logic blocks exchange data with an adjacent processing logic block only. Biemond simply discloses an image deblurring method which is not the same as the Applicant's and Nash discloses a systolic array processor. Biemond in view of Nash would produce the results of the Applicant's invention as the method of Biemond performed on the systolic array processor of Nash would not yield the results of iteration *within* a video frame update rate.

Additionally, Biemond does not disclose that the iterative update stores each pixel of the image in three planes within the systolic array processor as in the Applicant's FIG. 1. As disclosed in the Applicant's paragraph [0034], the Applicant's method utilizes data from a localized neighborhood of each pixel in each of three

planes; the blurred image, a prediction error and a deblurred image estimate. This is not disclosed in Biemond in view of Nash.

Biemond fails to disclose the limitation wherein the pixels arrive in each processing logic block of said array of processing logic blocks *respectively*. As the Examiner has admitted, Biemond does not disclose a systolic array processor and Nash does not disclose video image processing, how can the combination disclose that pixels arrive in the processing logic blocks respectively? The Examiner has not cited how this is disclosed in the references, and in fact, this limitation is not disclosed in either reference of the combination.

Therefore, Biemond in view of Nash fails in the aforementioned *prima facie* obviousness test as each and every limitation if the Applicant's claims are not disclosed. Biemond in view of Nash fails to disclose:

1) the image is a *video* image;

2) each processing block exchanges data *only* with adjacent processing blocks;

3) the iterative update stores each pixel of the image in three planes within the systolic array processor;

4) the iterative update occurs within a video frame update rate of the video image; and

5) the pixels arrive in each processing logic block of said array of processing logic blocks *respectively.*

The Applicant notes that the Examiner cited Biemond for disclosing "an" iterative method for image deblurring, yet does not specifically state that the method of Biemond discloses the Applicant's method. The Applicant agrees that Biemond discloses an iterative method for image deblurring, but it is not the same method utilized by the Applicant, as argued above. The MPEP states that among the

basic criteria to establish a *prima facie* case of obviousness, the teaching or suggestion of all the claim limitations by the prior art reference (or references when combined) is required.

The Applicant notes that the Examiner has further cited the Owens and Amin references in the Biemond in view of Nash rejections. The Applicant asks is this therefore actually a rejection over Biemond in view of Nash and further in view of *Owens* and *Amin*? The Applicant reminds the Examiner that the teaching or suggestion of all the claim limitations by the prior art references must be shown in the combined cited rejection references; i.e. Biemond and Nash. The Applicant submits that in this case it is not relevant as the Owens and Amin references do not disclose the limitations as discussed above.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 1, 7 and 14 based on Biemond in view of Nash be withdrawn.

Biemond et al. in view of Nash et al./Owens et al.

The Examiner rejected claims 5, 12, and 19 under 35 U.S.C. §103(a) as being unpatentable over Biemond and Nash in view of Owens et al. ("Computer Vision of the MGAP"), hereinafter referred to as "Owens".

Regarding claim 5, the Examiner argued that Biemond in view of Nash/Owens discloses the method of claim 1, wherein said processor groups pixel in groups that comprise at least one pixel. The Examiner argued that claims 12 and 19 claim the corresponding device that performs the method of claim 5. The Examiner argued that as per the rejection of claim 5, the device has been disclosed.

The Examiner argued that Biemond and Nash teach the deblurring of an image using a systolic processor but admitted that they do not discuss in detail how the pixels are grouped for processing. The Examiner argued that Owens teaches

the implementation of image processing methods using systolic array processors for image processing and (citing Owens, final line of the 2nd paragraph on page 338) that at a least one pixel is operated on per processor. Thus, the Examiner argued that as is evidenced by Owens one of ordinary skill in the art would have understood how to group the pixels for processing. The Examiner argued that it would have been obvious to one of ordinary skill in the art to combine Biemond and Nash with Owens to implement the image processing applications as were suggested by Nash.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1, 7 and 14 applies equally against the rejections of claims 5, 12 and 19 as these claims are dependent upon claims 1, 7 or 14.

Biemond in view of Nash and further in view of Owens therefore fails in the aforementioned prima facie obviousness test as each and every limitation of the Applicant's claims is not disclosed. Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 5, 12 and 19 based on Biemond in view of Nash and further in view of Owens be withdrawn.

Nash et al. in view of Biemond et al./Jagadish et al.

The Examiner rejected claims 2, 8, and 15 under 35 U.S.C. §103(a) as being unpatentable over Nash in view of Biemond and Jagadish et al. ("Array Architectures for Iterative Algorithms"), hereinafter referred to as "Jagadish".

Regarding claim 2, the Examiner argued that Nash in view of Biemond and further in view of Jagadish discloses the method of claim 1, wherein said processing logic blocks providing an iterative update of said blurred image by (i) providing feedback of the blurred image prediction error using the deblurred image and (ii) providing feedback of the past deblurred image estimate. The Examiner argued that

claims 8 and 15 claim the device corresponding to the method of claim 2. The Examiner stated that as per the rejection of claim 2 the device has been disclosed. .

The Examiner argued that Nash discloses the use of a systolic array for image deblurring as is disclosed in rejection of claim 1, but admitted that Nash does not disclose the particular method. The Examiner argued that Biemond discloses an iterative method for deblurring images (citing Biemond pages 865-868 under the section titled "C. Iterative Solutions". The Examiner cited in particular, equations 56 and 57 on page 865). Furthermore, the Examiner argued that as is evidenced by Jagadish (citing Jagadish sections 3-5) the implementation of iterative algorithms on a processing array were well known to one of ordinary skill in the art. The Examiner argued Jagadish discloses (citing Jagadish section 3) the procedure of obtaining the array architectures for iterative algorithms. (The Examiner further stated that Jagadish section 4 shows examples, and Jagadish section 5 discusses irregular cases.) The Examiner argued that it would have been obvious to one of ordinary skill in the art to combine Nash and Biemond given that it was known in the art to solve image deblurring using iterative methods (as taught by Biemond), and that it was known to use high performance processing arrays for deblurring (as taught by Nash) at the time of the invention. (The Examiner further cited the Abstract and Applications sections of Nash for the suggestion of using high performance, low complexity processing arrays for image deblurring.)

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejections of claims 1, 7 and 14 applies equally against the rejections of claims 2, 8 and 15 as these claims are dependent upon claims 1, 7 and 14.

The Applicant further notes that claim 2, 8 and 15 have been amended with this paper. Claim 2, for example is shown, as follows:

> The method of claim 1, wherein said three planes comprises said blurred video image, a blurred video image prediction error and a past deblurred video image

wherein said array of processing logic blocks provide said iterative update of said blurred video image by (i) providing feedback of said blurred image prediction error using said deblurred video image and (ii) providing feedback of said past deblurred image estimate.

The Applicant's FIG. 1 and paragraph [0034] disclose this limitation as argued above. The Nash, Biemond or Jagadish references do not disclose three planes within the systolic array processor wherein the three planes comprise the blurred video image, the blurred video image prediction error and a past deblurred video image.

Therefore, Nash in view of Biemond and further in view of Jagadish fails in the aforementioned prima facie obviousness test as each and every limitation of the Applicant's claims are not disclosed. Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 2, 8 and 15 based on Nash in view of Biemond and further in view of Jagadish be withdrawn.

Nash et al. in view of Biemond et al./Jagadish et al./Gorinevsky et al.

The Examiner rejected claims 3, 9-10, and 16-17 under 35 U.S.C. §103(a) as being unpatentable over Nash in view of Biemond, Jagadish, and Gorinevsky et al. ("Optimization-based Tuning of Low-bandwidth Control in Spatially Distributed Systems"), hereinafter referred to as "Gorinevsky".

Regarding claim 3, the Examiner argued that Nash in view of Biemond, Jagadish and Gorinevsky discloses the method of claim 2 wherein said iterative update is implemented in said processing logic blocks by $u(n + 1) = u(n) -- K *(H *u(n) -- y_b) -- S * u(n)$ where u is the ideal undistorted image, m and n are column and row indices of an image pixel element, $y_b (m,n)$ is the observed blurred image, * denotes a 2-D convolution, K is a feedback update operator with a convolution kernel $k(m,n)$ and S is a smoothing operator with a convolution kernel $s(m,n)$. The

Examiner argued that Biemond discloses $u(n + 1) = f(k+1)$, $u(n)=f(k)$, $g=y_b$, $K=B$ and *H-H* (the Examiner cited Biemond equations 56 and 57 on page 865).

The Examiner argued that Biemond identifies the existence of regularization error and discloses a solution of the regularization error (the Examiner cited Biemond section 5 which begins on page 868). The Examiner argued that the term S * u(n) as defined by applicant was known to one of ordinary skill in the art as a solution to the regularization problem. The Examiner admitted that Biemond does not teach the regularization method shown by the Applicant. However, the Examiner argued that Gorinevsky (citing Gorinevsky sections 1 and 3) teaches a filter that improves the spatial response (reduces regularization error) of the system. The Examiner argued that it would have been obvious to one of ordinary skill in the art to substitute the regularization method as taught by Gorinevsky for the regularization method taught by Biemond with a reasonable expectation of success while maintaining or improving the spatial response (reduction o[regularization error) provided by the method taught by Biemond Furthermore, the Examiner argued that in the same sections of Gorinevsky the use of the term K has also been disclosed.

Regarding claims 9 and 16, the Examiner argued that claims 9 and 16 claim the device corresponding to the method of claim 3. The Examiner argued that as per the rejection of claim 3, the device has been disclosed.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejections of claims 1, 7 and 14 applies equally against the rejections of dependent claims 3, 9 and 16. As submitted above, Biemond does not disclose:

1) the image is a *video* image;

2) each processing block exchanges data *only* with adjacent processing blocks;

3) the iterative update stores each pixel of the image in three planes within the systolic array processor;

4) the iterative update occurs within a video frame update rate of the video image; and

5) the pixels arrive in each processing logic block of said array of processing logic blocks *respectively.*

The inclusion of the Jagadish and Gorinevsky references does not disclose these limitations either. Therefore, Nash in view of Biemond, Jagadish, and Gorinevsky fails in the aforementioned *prima facie* obviousness test as each and every limitation of the Applicant's claims is not disclosed.

Furthermore, the Applicant submits that the equations cited by the Examiner in Biemond are not the same as disclosed and claimed by the Applicant. The addition of the cited equations in Gorinevsky does not result in the same equations as claims 3, 9 and 16. The Examiner has not provided a *prima facie* case of obviousness as the Examiner has not provided evidence that the combination results in the same equations as claimed.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 3, 9 and 16 based on Nash in view of Biemond, Jagadish, and Gorinevsky be withdrawn.

Regarding claims 10 and 17, the Examiner argued that Nash in view of Biemond, Jagadish, and Gorinevsky discloses the device of claim 9 and 16, wherein the operators H, K and S are preloaded in each of the array processing logic blocks. The Examiner admitted that Nash, Jagadish and Gorinevsky do not explicitly teach the preloading of the information into each processing logic block. However, the Examiner took official notice that it is notoriously known that in order to perform mathematical computations with these operators that these factors would have been initialized prior to performing the computations.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejections of claims 1, 7 and 14 applies equally against the rejections of dependent claims 10 and 17.

Furthermore, as the Examiner has admitted that Nash, Jagadish and Gorinevsky do not disclose preloading the operators into each processing logic block, the combination of the Nash, Biemond, Jagadish and Gorinevsky references does not disclose each and every limitation of the Applicant's claims. The Examiner has argued that it is well known in the art to initialize the factors prior to performing the computations. The Applicant agrees that the operators must be initialized before the computations are performed; however, that is not the limitation as claimed. The Applicant claims that the operators are *preloaded* into each processing logic block. This is disclosed in paragraph [0036] as follows:

> [0036] By accumulating the data within the reach demanded by the localized spatial operators in the update above for each pixel can be implemented within the respective processor. This presumes *preloading and storing* the operators H, K, and S in each of the array processing logic blocks. For each pixel the computations are extremely simple and require a number of additions, subtractions, and multiplications, proportional to the size (squared reach) of the FIR operators H, K, and S apart from the data transfer associated with downloading the blurred image and uploading the deblurred image estimate, the computational demand on each of the processing logic blocks does not at all depend on the image size. Of course, the overall amount of computations grows linearly with the image size. These computations are, however, performed in parallel by the processing logic blocks of the array. For large array size, an overall computational power of the described specialized parallel computer implemented by the systolic array could be very substantial. The data transfer requirements grow very slowly, as a square root of the image pixel size. Thus, the proposed approach is fully scalable and can be implemented at a very high speed for high resolution video images. Even for inexpensive systolic array processor, it is possible to do a few dozen update iterations within a video frame update time.

The Applicant submits that preloaded means that the operators are loaded into the processing logic blocks and stored therein for computations performed later. The operators H, K and S are preloaded before the image is downloaded. This is not "initialized" prior to performing the computations, as argued by the Examiner.

Therefore, the Applicant submits that Nash in view of Biemond, Jagadish and Gorinevsky fails in the aforementioned prima facie obviousness test as each and every limitation of the Applicant claims is not disclosed. Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 10 and 17 based on Nash in view of Biemond, Jagadish and Gorinevsky be withdrawn.

The Applicant furthermore respectfully requests that the Examiner provide the actual publication date of the Gorinevsky reference. The Gorinevsky reference includes two dates, only the first of which is a prior art reference under §103(a) based upon 102(b).

Nash in view of Biemond/Jagadish/Gorinevsky/Dowski

The Examiner rejected claims 4, 11 and 18 35 U.S.C. 103(a) as being unpatentable over Nash in view of Biemond, Jagadish, and Gorinevsky ("Optimization-based Tuning of Low-bandwidth Control in Spatially Distributed Systems") as applied to claims 3, 9-10, and 16-17 in further view of Dowski et al. (U.S. Patent Publication No. 2003/0169944), hereinafter referred to as "Dowski".

Regarding claim 4 the Examiner argued that the method of claim 4 is a modification of the method of instant claim 3 wherein the deblurring is performed on each color space separately. The Examiner argued that Biemond, Jagadish, and Gorinevsky discuss image processing, but admitted that they do not go into the particulars of color space processing. However, the Examiner argued that as is evidenced by Dowski (citing Dowski paragraph [0018]) the method of dividing an image into its color spaces and then deblurring each of the color spaces was known to one of ordinary skill in the art. The Examiner argued that the teaching of Dowski shows that one of ordinary skill in the art knew how to apply image-filtering processes such as deblurring to each color channel. The Examiner argued that given that Biemond at least teaches the deblurring of a grayscale image and that Dowski teaches the application of a single channel deblurring process to each of the color channels. The Examiner argued it would have been obvious to one of ordinary

skill in the art to combine the teachings of Dowski with Biemond to perform the deblurring technique as taught by Biemond on each channel of a color image and yield the expected result of a deblurred color image.

The Examiner argued that claims 11 and 18 claim the device corresponding to the method of claim 4. The Examiner argued that as per the rejection of claim 4 the device has been disclosed.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejections of claims 1, 7 and 14 applies equally against the rejections of dependent claims 4, 11 and 18. As submitted above, Nash in view of Biemond, Jagadish, and Gorinevsky does not disclose each and every limitation of the Applicant's independent claims. The addition of the Dowski reference does supply the limitations either.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 4, 11 and 18 based on Nash in view of Biemond, Jagadish, Gorinevsky and Dowski be withdrawn.

Nash in view of Owens

The Examiner rejected claims 6, 13, and 20 under 35 U.S.C. §103(a) as being unpatentable over Nash in further view of Owens ("Computer Vision on the MGAP").

Regarding claim 6, the Examiner argued that the method of claim 5 is disclosed by Nash in view of Owens, wherein said groups of pixels comprises a group selected from 2 by 2 pixels, 3 by 3 pixels, and 4 by 4 pixels. The Examiner argued that filtering and image processing methods such as deblurring are done locally by particular filter sizes depending on the desired outcome. The Examiner argued that Owens describes image processing using array processors (citing Owens section 3.1, page 338) disclosed the use of 3 x 3 masks applied to the image and hence the Examiner argued that it was known to group and process pixels in the 3 x 3 format in a processing array. The Examiner argued that it would

have been obvious to one of ordinary skill in the art to combine Nash and Owens to improve the utility and efficiency of the processing arrays by allowing local filtering operations to be performed on groups of pixels.

The Examiner argued that claims 13 and 20 claim the device corresponding to the method of instant claim 6. The Examiner argued that as per the rejection of instant claim 6, the device has been disclosed.

The Applicant respectfully disagrees with this assessment and notes that the argument presented above against the rejection of claim 1, 7 and 14 applies equally against the rejections of dependent claims6, 13 and 20.

Additionally, Owens discloses a 3 x 3 "mask" without disclosing that 3 x 3 groups of *pixels* arrive in *each* processing logic block of said array of processing logic blocks *respectively*. The Applicant's invention includes the limitation wherein groups of pixels arrive in the processing logic blocks respectively. Owens does not disclose this limitation and therefore Nash in view of Owens fails in the aforementioned prima facie obviousness test as each and every limitation of the Applicant's claims is not disclosed.

Based on the foregoing, the Applicant respectfully requests that the 35 U.S.C. §103(a) rejections of claims 6, 13 and 20 based on Nash in view of Owens be withdrawn.

II. Conclusion

In view of the foregoing discussion, the Applicant has responded to each and every rejection of the Official Action. The Applicant has clarified the structural distinctions of the present invention. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §103 based on the preceding remarks. Reconsideration and allowance of Applicant's application is also respectfully solicited. A Request for Continued Examination (RCE) under 37 CFR 1.114 is also submitted herewith, including the RCE fee of $810.

Should there be any outstanding matters that need to be resolved, the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

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